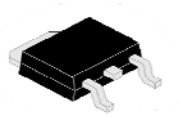
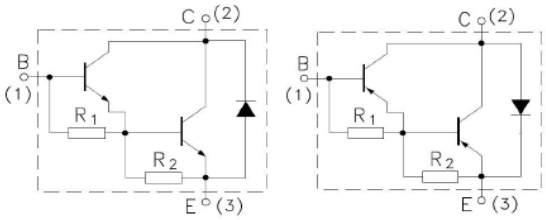
COMPLEMENTARY DARLINGTON PLASTIC POWER TRANSISTORS



DPAK (TO-252)

Internal Schematic Diagram



NPN: R1 ~ 8K Ohm
R2 ~120 Ohm

PNP R1 ~8K Ohm
R2 - 120 Ohm

MJD122 NPN
MJD127 PNP

DPAK (TO-252)
Plastic Package
RoHS compliant

APPLICATION:

Designed for General Purpose Amplifier and Low Speed Switching Applications

ABSOLUTE MAXIMUM RATINGS (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	VALUE	UNIT
Collector Base Voltage	V_{CBO}	100	V
Collector Emitter Voltage	V_{CEO}	100	V
Emitter Base Voltage	V_{EBO}	5	V
Collector Current Continuous	I_C	8	A
Collector Current Peak	I_C	16	A
Base Current	I_B	120	mA
Total Power Dissipation Tc=25ºC Derate Above 25ºC	P_D	20 0.16	W W/°C
Operating and Storage Junction Temperature Range	T_j, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Junction to Case	$R_{th\ (j\text{-}c)}$	6.25	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C; unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITION	VALUE			UNIT
				MIN.	TYP.	MAX.	
Collector Emitter Sustaining Voltage		V_{CEO}	I_C=30mA, I_B=0	100	--	--	V
Collector Cut Off Current		I_{CEO}	V_{CE}=50V, I_B=0	--	--	10	µA
Collector Cut Off Current		I_{CBO}	V_{CB}=100V, I_E=0	--	--	10	µA
Emitter Cut Off Current		I_{EBO}	V_{EB}=5V, I_C=0	--	--	2	mA
DC Current Gain		h_{FE}	I_C=4A, V_{CE}=4V	1000	--	12000	
			I_C=8A, V_{CE}=4V	100	--	--	
Collector Emitter Saturation Voltage		$V_{CE(sat)}$	I_C=4A, I_B=16mA	--	--	2	V
			I_C=8A, I_B=80mA	--	--	4	V
Base Emitter Saturation Voltage		$V_{BE(sat)}$ [1]	I_C=8A, I_B=80mA	--	--	4.5	V
Base Emitter On Voltage		$V_{BE\ (on)}$	I_C=4A, V_{CE}=4V	--	--	2.8	V
DYNAMIC CHARACTERISTICS							
Current Gain Bandwidth Product		F_T	V_{CE}=4V, I_C=3A, f=1MHz	4	--	--	MHz
Output Capacitance	**MJD127**	C_{ob}	I_E=0, V_{CB}=10V, f=0.1MHz	--	--	300	pF
	MJD122			--	--	200	

Note:

1. Pulse test: Pulse width ≤ 300ms, duty cycle ≤ 2%
2. For PNP type voltage and current values are negative.

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

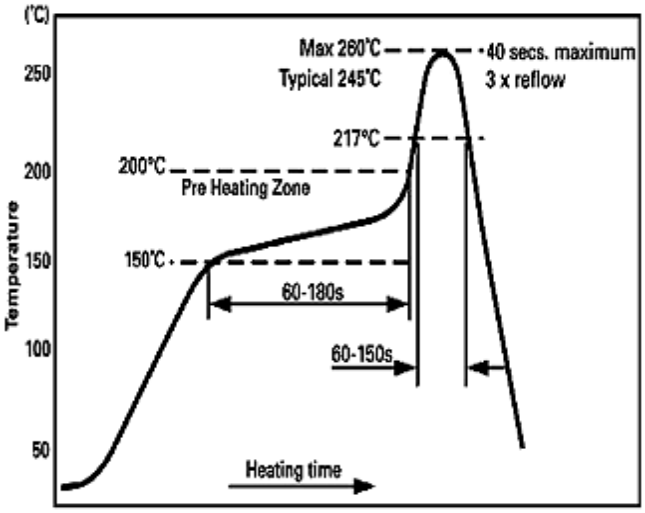
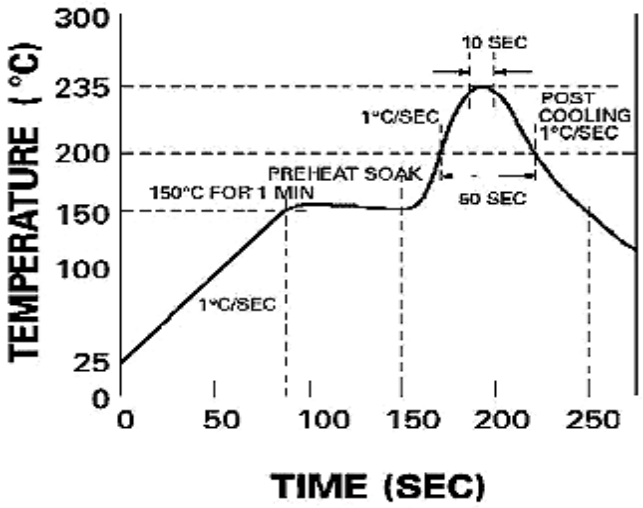


Figure 2

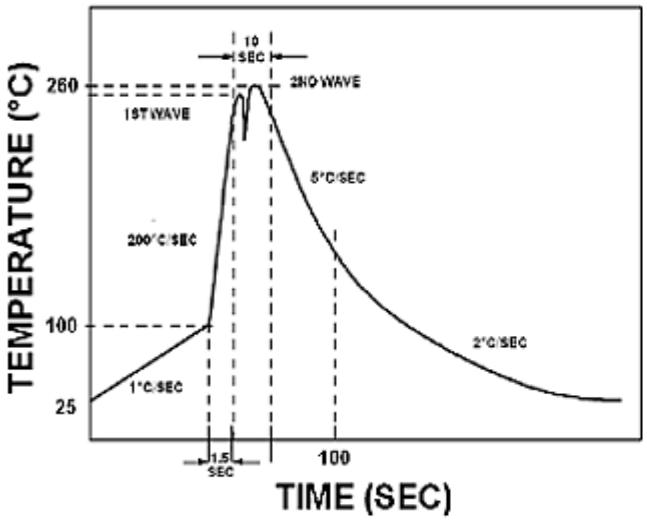


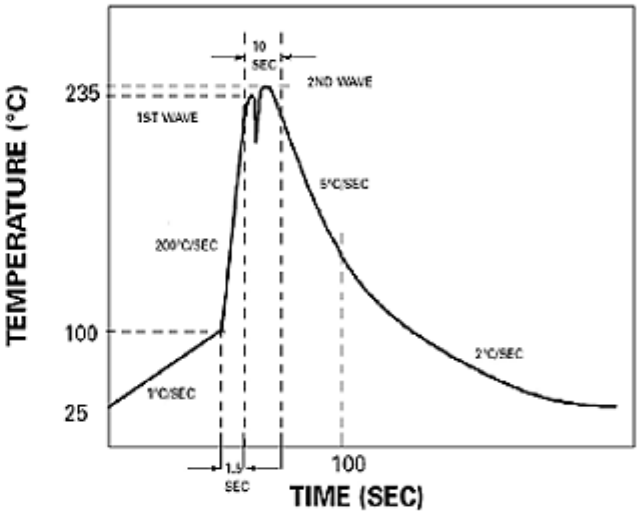
Reflow profiles in tabular form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used	The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder





Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

TYPICAL CHARACTERISTICS CURVES

Figure 1. Power Derating

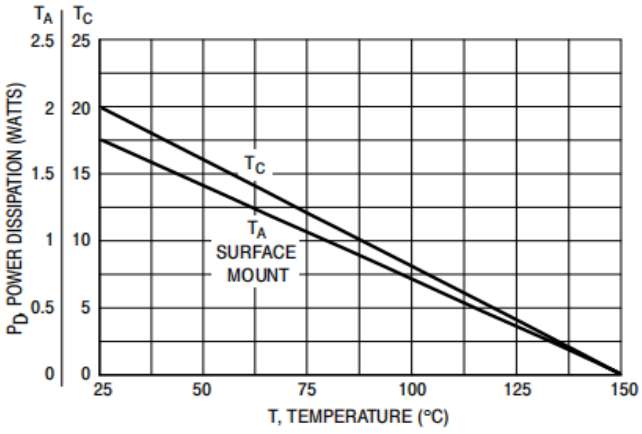


Figure 2. Maximum Forward Bias Safe Operating area

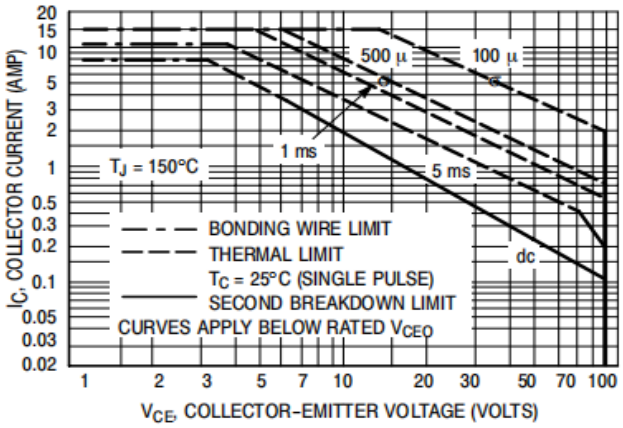
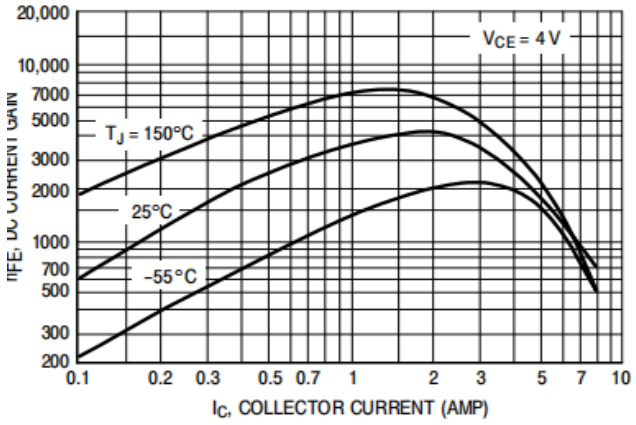


Figure 3. DC Current Gain

PNP MJD127



NPN MJD122

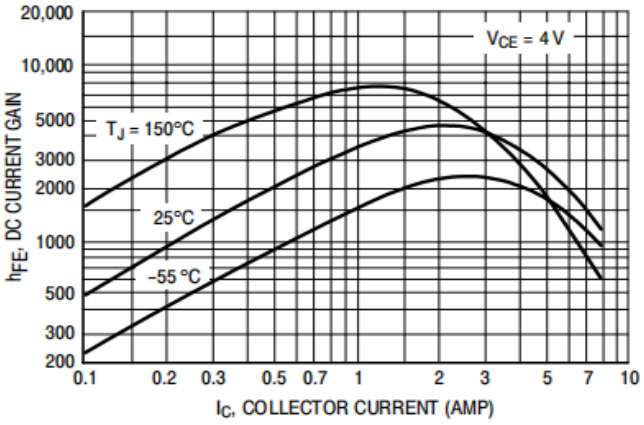
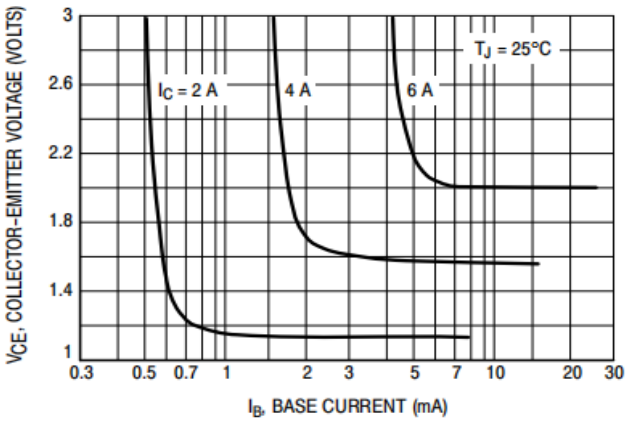
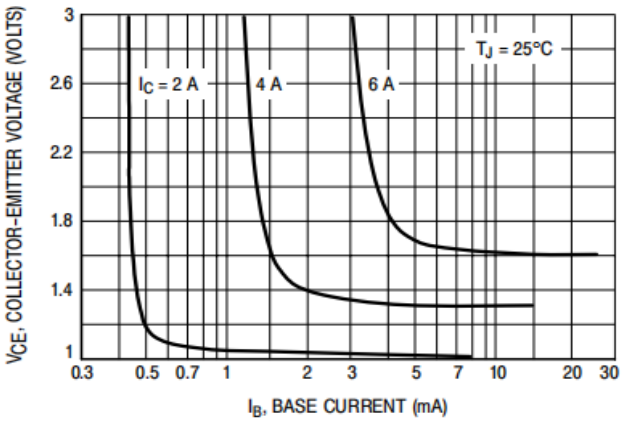


Figure 4. Collector Saturation Region

PNP MJD127



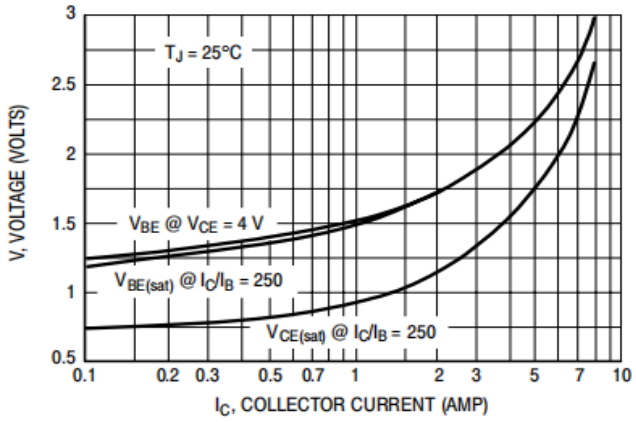
NPN MJD122



TYPICAL CHARACTERISTICS CURVES

Figure 5. “On” Voltages

PNP MJD127



NPN MJD122

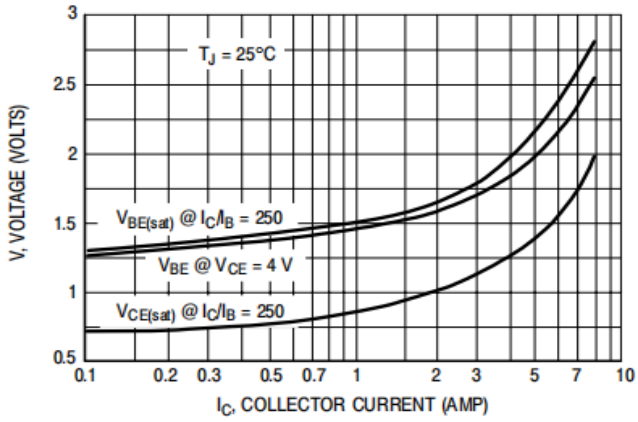
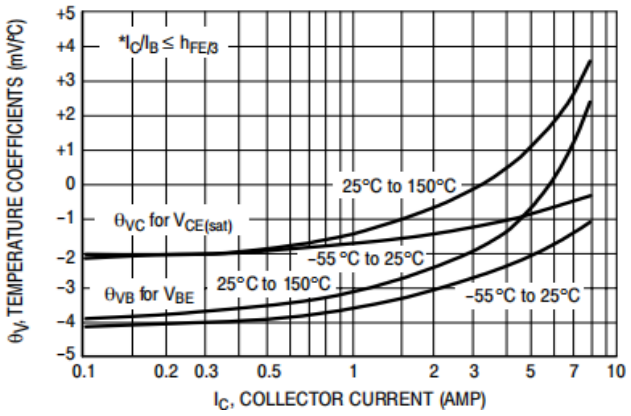


Figure 6. Temperature Coefficients

PNP MJD127



NPN MJD122

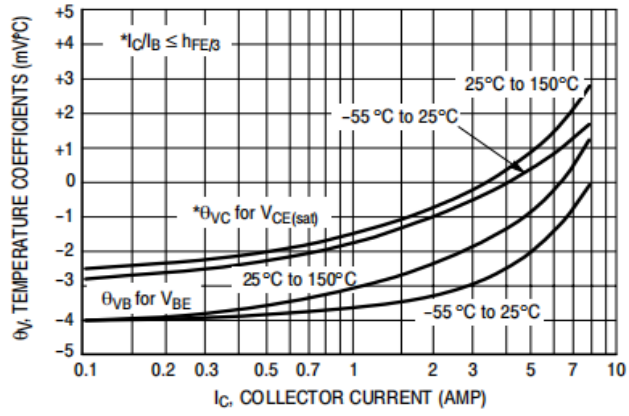
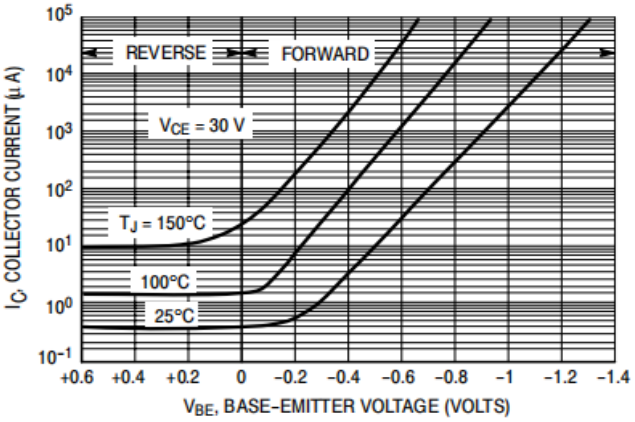
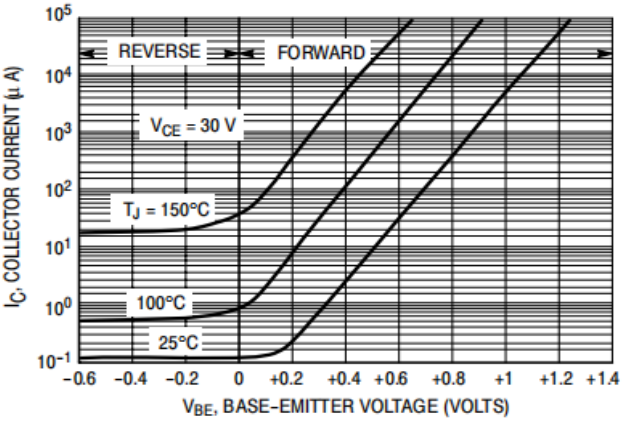


Figure 7. Collector Cut−Off Region

PNP MJD127



NPN MJD122



TYPICAL CHARACTERISTICS CURVES

Figure 8. Small−Signal Current Gain

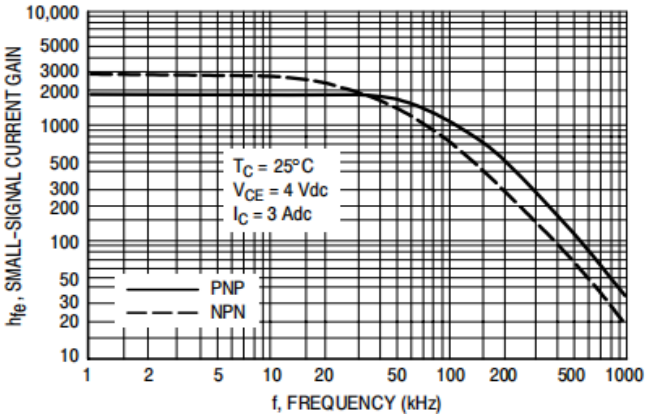


Figure 9. Capacitance

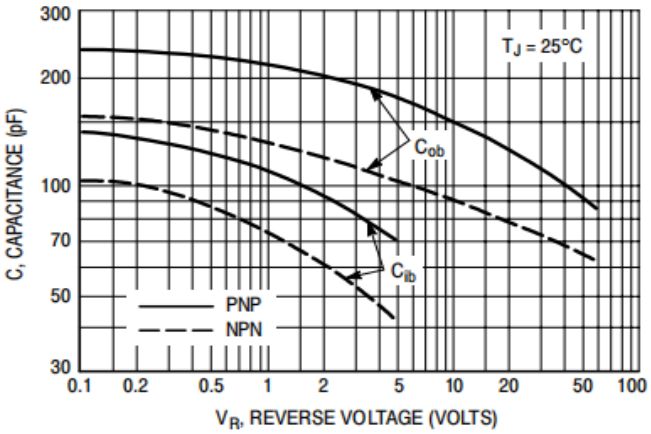


Figure 10. Switching Times Test Circuit

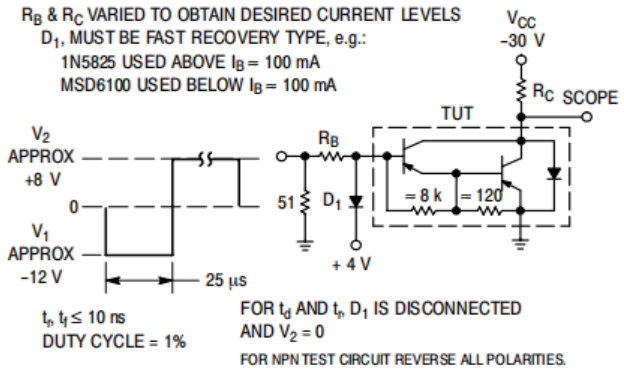


Figure 11. Switching Times

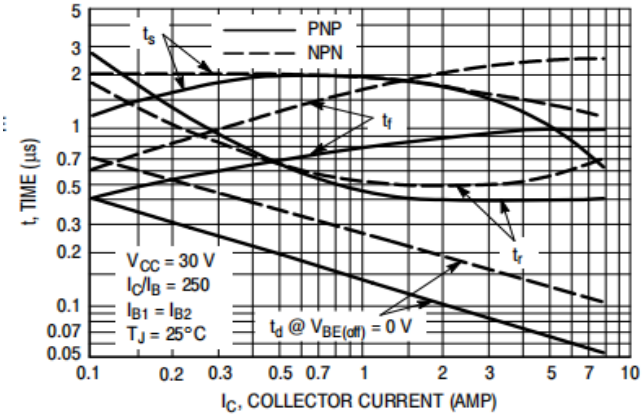
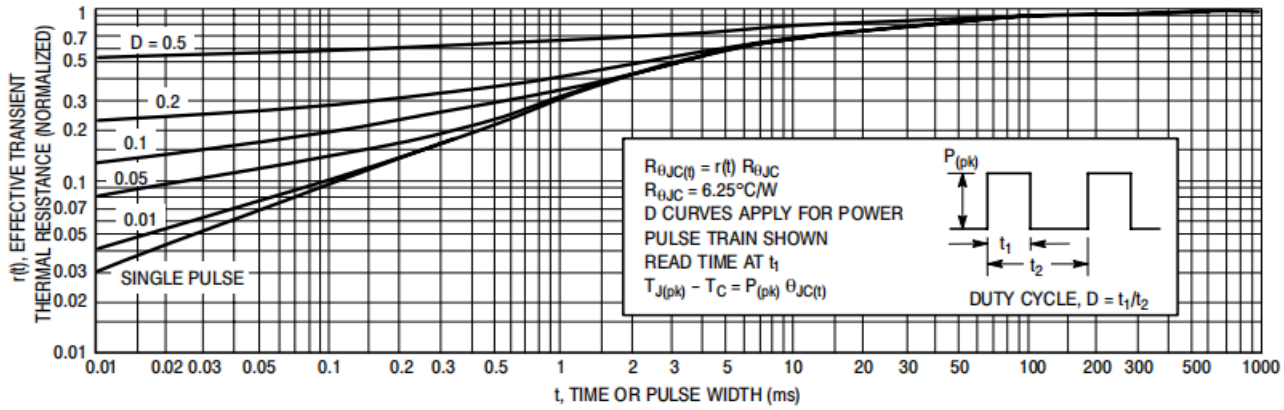
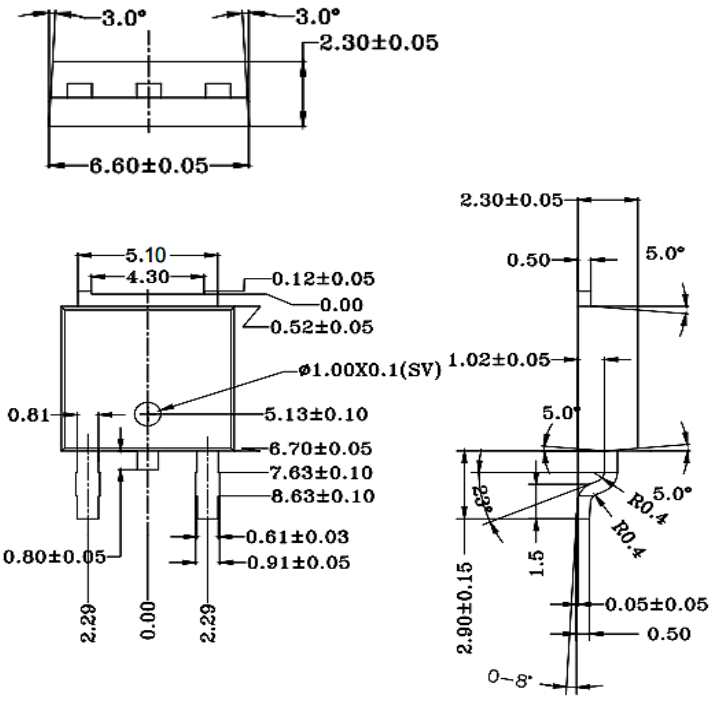


Figure 12. Thermal Response



PACKAGE DETAILS

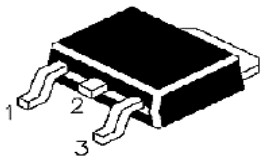
DPAK (TO-252) Plastic Package



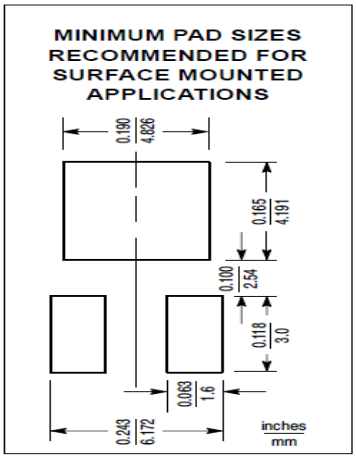
All dimensions are in mm

Pin Configurations:

1. Base
2. Collector
3. Emitter



PCB pads layout :



MJD122_127
Rev03 02072022EFC

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
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